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# Electron and hole mobilities at a Si/SiO<sub>2</sub> interface with giant valley splitting

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We examine the electron mobility and hole mobility at the Si/buried oxide (BOX) interface at which the valley splitting of the electron system is strongly enhanced, and compare the values observed to those at a standard Si/thermal oxide (T-SiO<sub>2</sub>) interface in the same silicon-on-insulator device. In contrast to the electron mobility, which is lower at the Si/BOX interface, the hole mobility at the Si/BOX interface is found to be slightly higher than that at the Si/T-SiO<sub>2</sub> interface.

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Electrons in a number of material systems such as bismuth, AlAs, MoS<sub>2</sub>, graphene, and silicon possess a valley degree of freedom arising from the degeneracy of their dispersion relations and valleytronics, in which this valley degree of freedom is exploited in addition to charge and spin in conventional electronic and spintronic devices and has become a subject of growing interest.<sup>1</sup> In silicon, understanding and becoming able to control the valley degree of freedom are of particular importance beyond their purely scientific value (for example, due to its role in the metal-insulator-transition<sup>2</sup>), because it has important consequences in relation to its future applications in quantum information processing,<sup>3–5</sup> and harnessing quantum mechanical and atomistic properties of silicon is becoming increasingly important, in general, with the imminence of the scaling limit.

In (001) silicon, there is a two-fold valley degeneracy arising from the two out-of-plane minima in the conduction band dispersion. The lifting of this degeneracy, known as valley splitting, has been observed experimentally and reported by many groups in Si Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs)<sup>6,7</sup> and Si/SiGe heterostructures.<sup>8</sup> Typical values are under a couple of meV and the effect is attributed to coupling across the two valleys mediated by the out-of-plane confining potential. Unexpectedly larger values of valley splitting are, however, observed at the Si/Buried OXide (BOX) interface in Si MOSFETs fabricated from Separation by IMplanted OXYgen (SIMOX) wafers.<sup>9</sup> Values of more than 20 meV can be readily achieved, indicating that the valley splitting is enormously affected by the characteristics of the interface and, suggesting that this could offer a powerful tool to manipulate and exploit the valley degree of freedom.

Theoretical considerations have demonstrated that the valley splitting is affected by atomic steps at the Si/barrier interface<sup>10</sup> and the details of the Si/barrier interface potential.<sup>11</sup> Furthermore, it is also proposed that extended interface states

can enhance the valley splitting to beyond tens of meV.<sup>12</sup> However, there is still no quantitative theory correctly predicting the magnitude of the valley splitting in these structures. A previous study had found that the resistivity of a 2D electron system at the Si/BOX interface is strongly enhanced under valley polarization, i.e., when the 2D electrons all reside within one valley sub-band.<sup>9,13</sup> However, it is unclear to what extent the origin of the resistivity enhancement is due to the valley polarization itself by a mechanism similar to resistivity enhancement with spin polarization,<sup>14</sup> or intrinsic disorder such as due to surface roughness scattering, which may be particularly adverse at this interface, limiting its potential usefulness for valley splitting control.

In this letter, in order to make a direct comparison between a standard interface with small valley splitting and an interface with giant valley splitting, we present measurements of the electron mobility and hole mobility at the two interfaces of the same device. Holes do not possess the valley degree of freedom and their behavior is not affected by it. We find that although the electron mobility at the Si/BOX interface is much lower than that at the standard Si/Thermal oxide (T-SiO<sub>2</sub>) interface, the hole mobility at the Si/BOX interface is slightly higher than that at the Si/T-SiO<sub>2</sub> interface. Furthermore, the out-of-plane potential confinement dependence of the hole mobility at the two interfaces roughly follows the expected form for surface roughness scattering,<sup>15</sup> where the out-of-plane potential confinement dependence at the Si/BOX interface is weaker. These findings show that for the holes, surface roughness scattering at the Si/BOX interface is weaker compared to that at the standard Si/T-SiO<sub>2</sub> interface strongly suggesting that the suppression of the electron mobility at the Si/BOX interface is not due to a particularly adverse magnitude of the surface roughness but dominated by the physics of valley polarization itself.

Our Si MOSFET is fabricated on a Silicon On Insulator (SOI) substrate made by the SIMOX process. The BOX layer, which is initially made by oxygen ion implantation and annealing at 1250 °C, is annealed further for a prolonged duration of 40 h at a higher temperature of 1350 °C in an argon-oxygen mixture. The top-gate oxide (T-SiO<sub>2</sub>) is made by thermal oxidation in dry oxygen ambient at temperature

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between 800 and 1000 °C. The thicknesses of the T-SiO<sub>2</sub>, SOI, and BOX layers are nominally 80 nm, 18 nm, and 380 nm, respectively. Previous atomic force microscopy studies of interfaces prepared in this way but exposed by selective chemical etching found the rms roughness values over wide (20 μm × 20 μm) areas to be 0.37 nm and 0.58 nm for the front and back interfaces, respectively.<sup>16</sup> Other estimates also point to a roughness of less than 1 nm for the two interfaces.<sup>17</sup> Figure 1(a) shows a TEM image of a quantum well (QW) cut from an identical device on the same wafer as those used for transport experiments presented in this paper. Routine TEM images of our structures, including Fig. 1(a), confirm that both interfaces are abrupt at a few-atom level, but it is not possible to see any conclusive quantitative differences in roughness between them in such images. The similarity in the scale of the interface roughness confirms that this is not responsible for the difference in valley splitting, and points to other possible differences such as interface morphology, i.e., the microscopic structural details of the roughness, or the nature of the interface at an atomic level.

A layer of polycrystalline silicon is deposited on the T-SiO<sub>2</sub> layer to serve as a front-gate electrode, while the substrate acts as a back-gate electrode (Fig. 1(b)). Source, drain, and Hall voltage electrodes were split into two and were doped independently with phosphorus and boron to form *n*- and *p*-type contacts, in order to measure the sheet resistivity of both 2D electrons and holes at the same interfaces in the same QW.<sup>18</sup> The longitudinal and transverse dimensions of the Hall bar are 10 μm and 8 μm, respectively. The resistivity  $\rho$  was measured with a standard low-frequency (13 Hz) lock-in technique while changing the electron and hole densities and potential asymmetry by applying front-gate and back-gate voltages. The sample was held in a cryostat and kept at a temperature of 5 K.

The front-gate voltage  $V_F$  dependence of the conductivity  $\sigma$  ( $= 1/\rho$ ) at a back-gate voltage  $V_B = 0$  V is shown in Fig. 2(a). Conduction at  $V_F > 0$  is due to electrons, whereas the conduction at  $V_F < 0$  is due to holes. Figure 2(b) shows a

two-dimensional plot of the conductivity as a function of both  $V_F$  and  $V_B$ . In order to separate the effects of the carrier density and potential confinement, we introduce two parameters, carrier density  $n$  and potential asymmetry  $\delta$

$$n = (n_B + n_F) = C_B(V_B - V_B^T)/e + C_F(V_F - V_F^T)/e,$$

$$\delta = (n_B - n_F) = C_B(V_B - V_B^T)/e - C_F(V_F - V_F^T)/e,$$

where  $n_{F,B}$  are carrier densities contributed by front (F) and back (B) gates, while  $V_{F,B}^T$  and  $C_{F,B}$  are corresponding threshold voltages and gate capacitances. These are determined from measurements of Shubnikov-de Haas oscillations at low temperature. Each of these parameters differs for the two carrier types. Axes for  $n_{e,h}$  and  $\delta_{e,h}$  are marked in Fig. 2(b).

Lines marked A (A') in Fig. 2(b) correspond to the onset of occupation of an upper electron (hole) confinement sub-band. These are also determined from Shubnikov-de Haas measurements showing distinctive beating patterns indicating the occupation of additional sub-bands.<sup>19</sup> In the data presented [Fig. 2(b)], the occupation of upper sub-bands can be

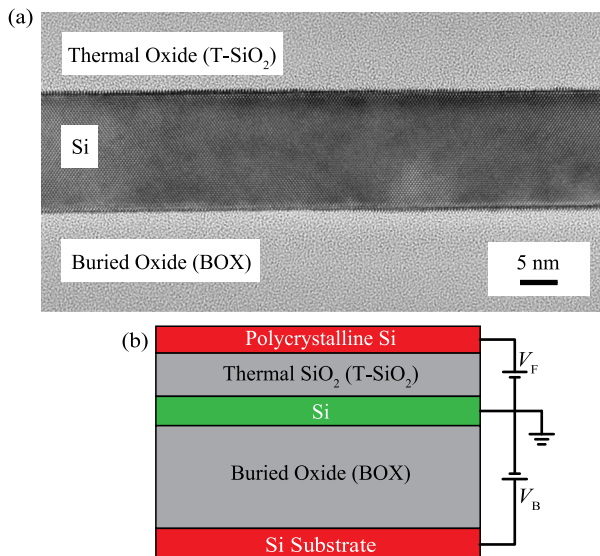


FIG. 1. (a) TEM image and (b) schematic diagram of the Si SIMOX MOSFET.

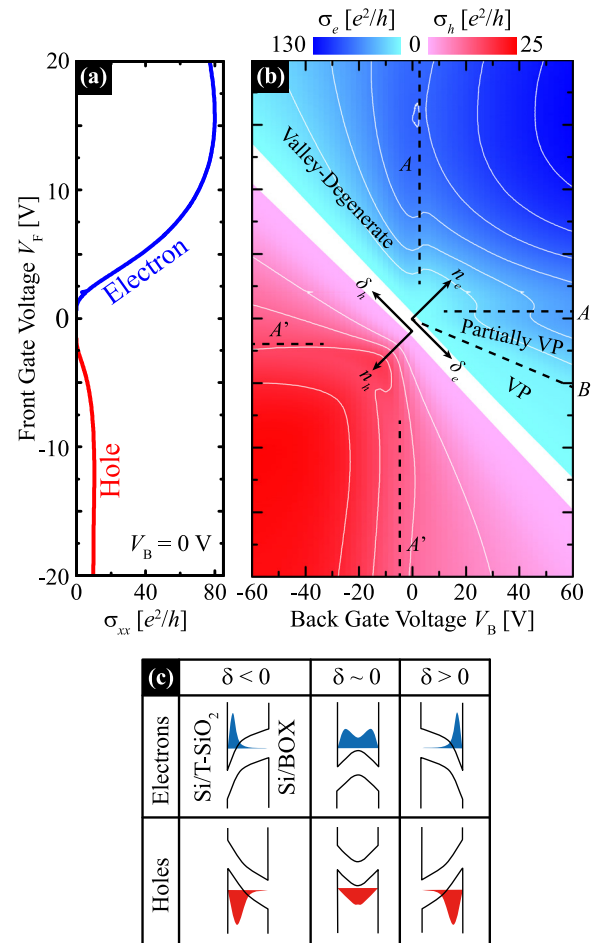


FIG. 2. (a)  $V_F$  dependence of the conductivity of electrons  $\sigma_e$  and holes  $\sigma_h$  at  $V_B = 0$  V and  $T = 5$  K. (b)  $\sigma_e$  and  $\sigma_h$  at  $T = 5$  K as a function of  $V_F$  and  $V_B$ . Lines A and A' indicate the positions of the onset of the upper spatial sub-band. The valley-polarized region is labelled VP and a line B marks the boundary between the valley-polarized and partially valley-polarized regions. The axes in the figure show the carrier density  $n$  and potential asymmetry  $\delta$ . (c) Schematic diagram of the potential asymmetry and carrier distribution in the quantum well. The potential asymmetry and total carrier density can be changed by the two gate electrodes.

seen by the suppression of the conductivity along these lines A and A'. Occupation of low mobility states at the bottom of the upper sub-band and abrupt changes in intersub-band scattering and screening<sup>6</sup> result in these features demarcating sub-band edges.

The Shubnikov-de Haas oscillations also allow us to determine the valley splitting. When the electrons are pressed against the Si/BOX interface (positive  $\delta$ , Fig. 2(c)), the valley splitting  $\Delta$  is found to increase in proportion to  $\delta$  ( $\Delta = \alpha\delta$ ) as observed previously<sup>9</sup> with comparable values, where  $\alpha = 4.4 \times 10^{16} \text{ meV m}^{-2}$  gave the best fit for this sample. For example, this gives  $\Delta = 22 \text{ meV}$  for  $\delta = 5 \times 10^{16} \text{ m}^{-2}$ . On the other hand, when  $\delta$  is negative (electrons at the Si/T-SiO<sub>2</sub> interface), the valley splitting is too small to be quantified by this technique and there is no reason to suppose that it does not behave in a similar manner as at standard interfaces, as previously described,<sup>19</sup> where the value remains below a couple of meV within the gate-voltage range studied. A region in which only one valley sub-band is occupied, i.e., the electrons are fully valley polarized, is marked VP in Fig. 2(b).

Figures 3(a) and 3(b) show the electron mobility  $\mu_e$  for  $\delta_e < 0$  and  $\delta_e > 0$ , respectively, obtained from the data in Fig. 2(b) using the relation  $\mu_e = \sigma_e / en_e$ .  $\mu_e$  is suppressed when  $\delta_e$  is small [Figs. 3(a) and 3(b)] for both  $\delta_e < 0$  and  $\delta_e > 0$  due to the effects of the upper spatial sub-band,<sup>6</sup> and this feature disappears as  $|\delta_e|$  increases due to the out-of-plane potential raising the confinement energy of the upper spatial sub-band with respect to the ground sub-band. In this letter, we focus on the transport properties where only one spatial confinement sub-band is occupied.

When  $\delta_e$  is large and negative, the electrons are pressed against the Si/T-SiO<sub>2</sub> interface. Below  $\delta_e \sim -2 \times 10^{16} \text{ m}^{-2}$  [Fig. 3(a)],  $\mu_e$  begins to decrease as  $\delta_e$  decreases and below  $\delta_e \sim -4 \times 10^{16} \text{ m}^{-2}$ ,  $\mu_e$  obeys a power law where the exponent is close to  $-2$ . For example, a fit to data over this range with  $n_e = 0.6 \times 10^{16} \text{ m}^{-2}$  gives a power of  $-2.1$ , strongly suggesting the dominant role of surface roughness scattering in limiting the mobility. Previous work on conventional MOSFET structures has found mobility limited by surface roughness scattering at low temperature to be approximately described by  $\mu_{\text{SR}} \propto E_{\text{eff}}^{-2} / S(2k_F)$ , where  $E_{\text{eff}} = e(N_{\text{dpl}} + \eta N_s) / \epsilon_{\text{Si}}$  is the effective electric field

perpendicular to the 2D system,<sup>20,21</sup>  $N_{\text{dpl}}$  is the depletion charge density,  $N_s$  is the carrier density,  $\epsilon_{\text{Si}}$  is the permittivity of Si, and  $\eta$  is a fitting parameter with values of around  $\eta = 1/2$  for electrons and  $\eta = 1/3$  for holes.<sup>20,21</sup> In our device, the electric field in the two binding oxide layers is simply proportional to  $n_B$  and  $n_F$  so that at large  $|\delta|$ , where the potential approximates to a triangular potential, the equivalent effective field  $E_{\text{eff}}$  is proportional to  $\delta$ .  $S(k)$  is the power spectral density of the disorder potential, which is the Fourier transform of the spatial surface roughness distribution, and  $k_F$  is the Fermi wave vector. Thus, when the electron density is held constant,  $S(k_F)$  remains constant and the mobility limited by the surface roughness scattering is proportional to  $\delta^{-2}$ . In practice, a range of values between  $-1$  and  $-2.6$  for the exponent are observed<sup>21</sup> and our observation is comfortably consistent. The mobility is limited by surface roughness scattering when the electrons are pressed against the Si/T-SiO<sub>2</sub> interface as usual.

When the electrons reside at the Si/BOX interface ( $\delta_e > 0$ , [Fig. 3(b)]), the behavior is very different. The electron mobility  $\mu_e$  decreases more rapidly with increasing  $\delta_e$  and is followed by a kink structure marked by arrows in Fig. 3(b). The kink shifts to larger values of  $\delta_e$  with increasing density  $n_e$ , corresponding to the boundary between partially valley-polarized and valley-polarized regions. In the valley polarized region, the mobility is strongly suppressed in comparison to the mobility at negative  $\delta_e$  under equivalent conditions.

When the system is only partially valley polarized, the change of mobility with  $\delta_e$  is complicated by changes in  $k_F$  and the change in density of states with valley polarization as well as the change in the surface roughness scattering. However, within the valley polarized region, applying the same arguments would lead us to expect a mobility, which varies as  $\delta_e^{-2}$ . Attempting to fit power laws between  $\delta_e = +5.0 \sim +4.0 \times 10^{16} \text{ m}^{-2}$  gives values of  $-1.1$ ,  $-0.9$ , and  $-0.8$  for the exponents at  $n_e = 0.6, 0.8$ , and  $1.0 \times 10^{16} \text{ m}^{-2}$ , respectively, and clearly do not follow  $\delta_e^{-2}$ . We suspect that this relates to the proximity of the Fermi energy to the upper valley sub-band edge and that the  $\delta_e$  dependence is heavily influenced by the depopulation of the disorder broadened sub-band tail<sup>13</sup> but a detailed explanation remains for future work. At the largest values of  $\delta_e$ , the slope appears to become stronger [Fig. 3(b)], and this may signify a transition to the usual  $\delta_e^{-2}$  dependence, where the increase in interface roughness eventually becomes the dominant factor.

We now present data for holes measured at the same interfaces in the same device. Figure 4 shows the  $\delta_h$  dependence of the hole mobility  $\mu_h$ . In the same manner as for electrons, holes reside at the Si/BOX interface for  $\delta_h > 0$ , and at the Si/T-SiO<sub>2</sub> for  $\delta_h < 0$ . In stark contrast to the electron mobility, the hole mobility does not display dramatically large asymmetry between positive and negative  $\delta_h$ . Instead, the behavior is relatively symmetric, only showing slight differences. For all values of  $n_h$  and  $|\delta_h|$ , the hole mobility is slightly higher when  $\delta_h$  is positive indicating that the effects of disorder are weaker at the Si/BOX interface.

The mobility is a function of the effective mass as well as the relaxation time, and the effective mass of holes is affected by band modifications due to interactions between light and

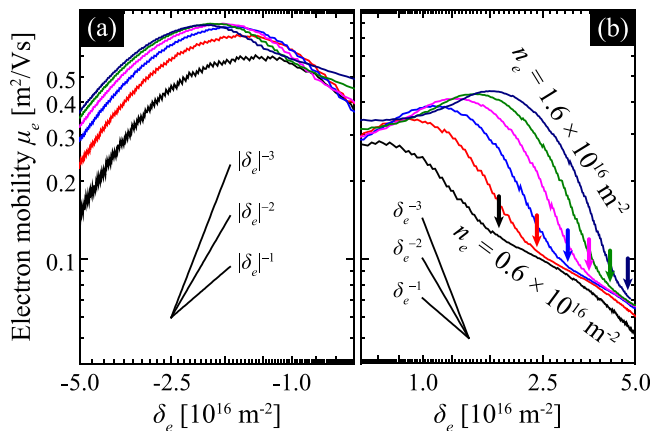


FIG. 3. Electron mobility for  $\delta_e < 0$  (a) and  $\delta_e > 0$  (b) at a temperature of 5 K. The electron density  $n_e$  is evenly stepped between  $0.6$  and  $1.6 \times 10^{16} \text{ m}^{-2}$ .



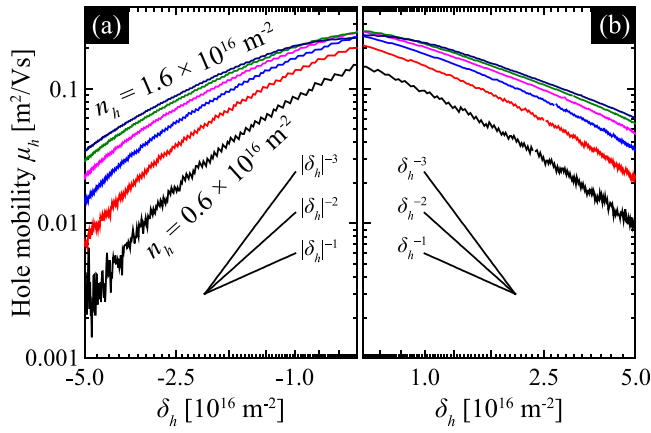


FIG. 4. Hole mobility for  $\delta_h < 0$  (a) and  $\delta_h > 0$  (b) at a temperature of 5 K. The electron density  $n_h$  is evenly stepped between  $0.6$  and  $1.6 \times 10^{16} \text{ m}^{-2}$ .

heavy hole states<sup>6</sup> which, in turn, are affected by the confinement  $\delta_h$ . However, we have performed Shubnikov-de Haas measurements, which confirm that this effect is symmetrical with respect to  $\delta_h$ , indicating that the symmetrical mobility we see does indeed reflect the comparable strength of disorder experienced by the holes at the two interfaces. The confinement dependence ( $|\delta_h|$  dependence) of  $\mu_h$  at large  $|\delta_h|$  is fairly close to  $\mu_h \sim \delta_h^{-2}$  at both interfaces showing that the dominant mechanism of scattering is surface roughness scattering for both interfaces. Agreement to the  $\mu_h \sim \delta_h^{-2}$  law is very good at the conventional Si/T-SiO<sub>2</sub> interface (exponent =  $-2.4$  between  $\delta_h = -5.0$  and  $-4.0 \times 10^{16} \text{ m}^{-2}$ ,  $n_h = 0.8 \times 10^{16} \text{ m}^{-2}$ ), while the Si/BOX interface shows a slightly more gentle slope [Fig. 4] (exponent =  $-1.6$  between  $\delta_h = 4.0$  and  $5.0 \times 10^{16} \text{ m}^{-2}$ ,  $n_h = 0.8 \times 10^{16} \text{ m}^{-2}$ ).

Comparing the  $\delta$  dependences of the mobility for electrons and holes [Figs. 3 and 4], only the electron mobility at the Si/BOX interface ( $\delta_e > 0$ ) deviates strongly from the  $\delta^{-2}$  law accompanied by the kink structure at the onset of valley polarization. This result indicates that the suppression of  $\mu_e$  at the Si/BOX interface is not dominated by surface roughness scattering, but is likely to be due to the valley polarization itself. The suppression of mobility in the valley-polarized and partially valley-polarized regions may be accounted for by the changing scattering rate due to the Fermi wave vector, Fermi energy, and density of states.<sup>14</sup> Indeed, the shallower  $\delta_h$  dependence of the hole mobility at this interface may also be pointing to qualitatively different disorder compared to the standard Si/T-SiO<sub>2</sub>, which may be a reflection of the differences leading to the giant valley splitting.

In summary, we have performed electron and hole transport measurements in a single SiO<sub>2</sub>/Si/SiO<sub>2</sub> QW fabricated from a SIMOX SOI wafer and evaluated the contribution of interface roughness scattering to the electron and hole mobility. In contrast to the electron mobility, which is strongly suppressed at the Si/BOX interface with giant valley splitting, the hole mobility shows higher values compared to the standard Si/T-SiO<sub>2</sub> interface. This strongly suggests that the suppression of the electron mobility at the Si/BOX interface is not due to a particularly adverse magnitude of the surface roughness but dominated by the physics of valley polarization itself.

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